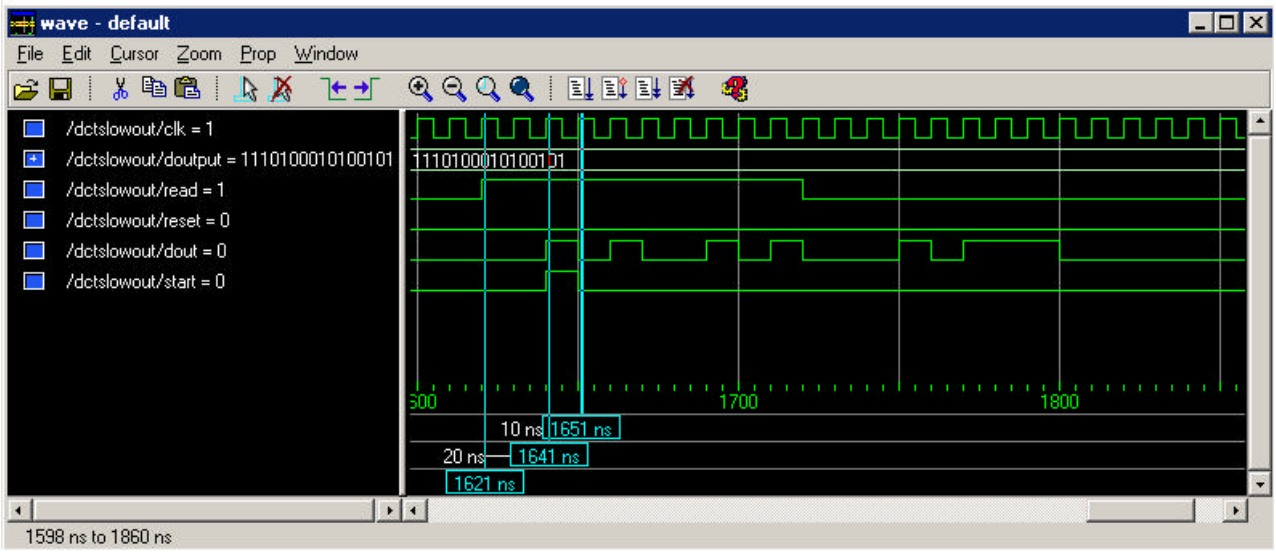
Parallel to Serial Output Converter

The file **serout.vhd** contains an entity **dctslowout**, which is an add-on to the **DCT8_slow** component. It converts the parallel output of **DCT8_slow** to a stream of serial bits. To achieve this, just connect the two blocks in the following configuration:

DCT8_slow (outputs)	Connects to	**dctslowout** (inputs)
read		**read**
doutput		**doutput**

Timing diagram



Examining the previous timing diagram, at the rising edge of **read** (*the first cursor at 1621ns*) the parallel word is transferred to **dctslowout**. After two clock cycles (*the second cursor at 1641ns*) the **start** output signal is asserted and so is the least significant bit of the output word. The value of the bit could be read properly after one clock cycle (*the third cursor at 1651ns*). The **clk** and **reset** inputs are connected to the global clock and reset terminals respectively, and as usual the circuit must be reset initially for proper operation. **reset** is active '1'.